

Notes on the operational frequency and programming of the NT2903/4 -

Choice of RF frequency

Specifications are written for the 902 to 928MHz ISM band. However the transmitter or receiver can be used with RF frequencies from 130MHz to 1000MHz by suitable choice of external inductor for the receiver and transmitter oscillator tank circuits. Approximate centre frequency calculations are given below.

$$\text{Tx VCO} \quad f = 1/(2\pi\sqrt{(L+L_p)*4.6\text{pF}})$$

$$\text{Rx VCO} \quad f = 1/(2\pi\sqrt{(L+L_p)*1.7\text{pF}})$$

[Note Rx VCO is 2x Rx RF local oscillator]

L is the external inductance to VDDT or VDDR from both the true and inverse tank outputs.
Lp is the effective package and bond wire inductance for both true and inverse tank outputs.
Lp = 2.6nH for the 48pin TQFP. This calculation assumes negligible external capacitance.

Assuming a $\pm 5\%$ tolerance on L, the guaranteed oscillator range is 3% of the centre frequency if the external inductor is set for devices from the centre of the distribution. Devices at the edge of the distribution can be brought to the correct centre frequency by selection of the appropriate oscillator trim. The Tx trim is programmed by bits 21, 22 and 23 of the transmitter frequency register; the Rx trim is programmed by bits 21 and 22 of the receiver frequency register.

The VCO gains will be between 2% and 4% of the total range per volt of the control voltage.

Choice of receiver bandwidth

The application circuit diagram is given for a 900MHz ISM band receiver with a 130kHz bandwidth. The chip is designed to be adjusted for bandwidths from 16kHz to 150kHz in the ISM band. Lower RF frequencies can be chosen some of the bandwidth setting adjustments scale with the RF frequency. There are 2 major elements to the receiver bandwidth: -

1. **BWbb**: the baseband bandwidth. This is defined by 8 pole low pass filters in both the I and Q baseband channels. The filtering in each channel is achieved by a two pole Sallen and Key filter combined with and a six pole Gm filter. The defining resistors and capacitors for the Sallen and Key filters are off chip; the Gm filter is totally on chip except for one bandwidth trimming resistor. Note that the bandwidth of the individual channels is $0.5 \cdot \text{BWdm}$.
2. **BWdm**: the demodulator bandwidth. This is the bandwidth of the Period to Digital demodulator. It is a 'brick wall' filter centred on the IF frequency.

Additional filtering issues: -

3. The DC offset correction feedback loop in the baseband section introduces an effective high pass filter in the centre of the RF band.
4. There is filtering in the IF section following the second mixer designed to attenuate mixer products before the demodulator. Filtering is defined by a 4 pole low pass filter followed by a single pole high pass filter. The low pass filter is an on chip Gm design with an off chip bandwidth trimming resistor and the high pass filter is on chip and fixed frequency.

Bandwidth adjustment

A. Sallen and Key baseband filters

The R and C components for this filter are off chip. To set the baseband bandwidth, BW_{bb}, adjust the C values. Choose values to give the a bandwidth equal to or slightly greater than the required bandwidth according to the following formulae.

The capacitor attached to IFIL2/QFIL2 = $1.8nF \cdot (130kHz/BW_{bb})$.

The capacitor attached to IFIL3/QFIL3 = $0.68nF \cdot (130kHz/BW_{bb})$.

E.G., for a required 32kHz bandwidth suggested values of 6.8nF and 2.6nF give a bandwidth of 34kHz.

B. Gm baseband filter

On chip baseband filter bandwidth is adjusted by choice of the external resistor between V_{DD}B and BBSET. Choose this resistor to give a bandwidth calculated from A. above.

$R = 22k\Omega \cdot (130kHz/BW_{bb})$.

E.G., for 34kHz bandwidth suggested value is 82k Ω .

C. Demodulator

Demodulator bandwidth, BW_{dm}, is adjusted by the choice of the Period to Digital demodulator clock frequency, F_{pd}. The chip divides down the receiver local oscillator, Fr_f, by the divide ratio, PDR, to obtain F_{pd}. PDR is programmed by bits 14, 15 & 16 of the reference frequency register. Allowable PDR ratios are 2¹, 6², 12, 24, 36, 48, 72, 96.

The choice of F_{pd} directly sets the IF frequency, F_{if}, and BW_{dm}: -

$F_{pd} = Fr_f/PDR$ $F_{if} = F_{pd}/544$ $BW_{dm} = F_{pd}/580$

Choose a value of PDR to give BW_{dm} > BW_{bb}.

¹Ratio 6 can only be used with Fr_f < 520MHz

²Ratio 2 can only be used with Fr_f < 180MHz

Examples

Fr _f , MHz	PDR	F _{pd}	F _{if}	BW _{dm}
915	12	76.25MHz	140.2kHz	131.5kHz
930	48	19.4MHz	35.6kHz	33.4kHz
430	6	71.7MHz	131.7kHz	123.6kHz

The second example in the table fits with the example used in A. and B.

D. IF filter

The bandwidth of the on chip IF low pass filter which precedes the Period to Digital demodulator should be optimised as follows. Following the calculation of F_{if} and BW_{dm} from C. above, the filter bandwidth is adjusted by choice of the external resistor between V_{DD} and BBSET.

$R = 22k\Omega \cdot 206kHz/(F_{if} + 0.5 \cdot BW_{dm})$.

E.G for F_{if}=35.6kHz, BW_{dm} = 33.4kHz optimum bandwidth is 53kHz, therefore choose R=86K Ω .

The on chip high pass filter is fixed at 8kHz.

E. Effective high pass baseband filter

The 3dB bandwidth is set to $\pm 100Hz$ by the external 330nF capacitors connected to DCI and DCQ. Adjustment by increasing the capacitor value in inverse proportion to the chose BW_{dm} is possible. Reduction in the cut of with BW_{dm}=130kHz may lead to instability in the Auto Gain set mode.

$(F_{if}) = \frac{F_{pd}}{2 \times 18 \times 16} \text{ (NT2903) (576)}$
 $(17)?$

Receiver Gain switching

The receiver includes a facility to switch the gain to maintain linearity over a wide range of on channel signal levels. This can be done manually via the 3 wire programming interface or automatically via an on-chip signal level measurement. The choice of manual or auto setting of the receiver gain is controlled by bit 3 of the Mode Register.

In manual mode: -

- A. There is a 10dB RF pad that can be switched in before the RF input mixers
 - B. The RF mixer gain can be cut by 10, 20 or 30dB
 - C. The baseband gain can be cut by 10, 20, 30 or 40dB
- See section on the Mode register for details of programming.

In auto mode: -

Gain switches to maximum following any change made to the information in the programming registers. The gain then switches automatically according to the measured signal level.

The received on channel signal is integrated in the baseband section before the second mixer. The signal integration time constant, T_{si} , can be altered externally by changing the value of the capacitor, C_{GCC} attached to the pin GCC.

$$T_{si} = 27ms * (C_{GCC}/330nF).$$

The integrated signal level is evaluated at intervals T_{se} . T_{se} is programmed by bits 21 & 22 of the Mode Register. The available T_{se} values increase with the demodulator bandwidth allowing for the signal evaluation over a similar number of baseband cycles of an on channel signal. Possible values of T_{se} are: -

- Tse1 7ms * (130kHz/BWdm)
- Tse2 14ms * (130kHz/BWdm)
- Tse3 28ms * (130kHz/BWdm)
- Tse4 56ms * (130kHz/BWdm)

At the end of an evaluation interval, the receiver gain is left unchanged or stepped up or down by one notch according to the table below: -

Nominal RF Signal Level		Voltage Attenuation dB					
		RF section		Baseband section			
Increasing	Decreasing	RF pad	RF Mixer	1st Block	2nd Block	3rd Block	4th Block
	< -92dBm	0	0	0	0	0	0
> -86dBm	< -82dBm	0	0	0	10	0	0
> -76dBm	< -72dBm	0	0	0	10	10	0
> -66dBm	< -62dBm	0	10	0	10	10	0
> -56dBm	< -52dBm	0	10	10	10	10	0
> -46dBm	< -42dBm	0	20	10	10	10	0
> -36dBm	< -32dBm	0	20	10	10	10	10
> -26dBm	< -22dBm	10	20	10	10	10	10
> -16dBm		10	30	10	10	10	10

Recommendations for setting Tsi and Tse

Tsi must be greater than the sum of the time necessary for: -

1. the baseband DC offset loop to slew to the linear region, fixed internally according to BWdm
2. settling time of the baseband DC offset loop; loop bandwidth is 100Hz
3. integration time for the signal; ~300 cycles of the maximum in band signal within the baseband section.

Recommended value for Tsi is: -

$$0.9\text{ms} \cdot (130\text{kHz}/\text{BWdm}) + 1.6\text{ms} + 4.5\text{ms} \cdot (130\text{kHz}/\text{BWbb})$$

Recommended value for Tse is

$$>2x \text{ Tsi}$$

If the channel is changed and the received signal is very strong necessitating a change from maximum gain to minimum gain the time taken will be $8 \times Tse$.

E.G.1 For 130kHz BWbb; Tsi = 7ms;

Tse = >14ms, choose Tse2 which gives Tse=14ms for BWdm = 130kHz

Change from maximum to minimum gain 110ms.

E.G.2 For 16kHz BWbb; Tsi = 45ms;

Tse = >45ms, choose Tse1 which gives Tse=56ms for BWdm = 16kHz.

Change from maximum to minimum gain 450ms.

Received Signal Strength Indicator

Recommended 10nF external capacitor attached to RSSI gives a 20% accuracy for the received power measurement with a 130kHz bandwidth receiver. For a narrower bandwidth receiver the capacitor may need to be increased to integrate the received power over a longer time.